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# Charge Current Controlled Single Phase Integrated Switched Mode Power factor Correction Converter

Mr.Mopidevi. Subbarao<sup>a</sup>\*, Dr.Ch.Sai Babu<sup>b</sup>, Dr.S.Satyanarayana<sup>c</sup>

<sup>a</sup>. Asst. professor in Dept. of EEE, VFSTR University, Vadlamudi. India <sup>b</sup>. Professor in Dept. of EEE, College of Engineering JNTUK, Kakinada. India <sup>c</sup> Principal Tenali Engg. College, Tenali. India

### Abstract

Integration of converters reduces the number of control switches and increases the power handling capacity. Charge current control have the features like fast dynamic response, design of compensator is easy and low switching noise, so this controller is applicable for power factor correction application. In this paper analysis, design and implementation of charge current controlled integrated buck flayback converter is proposed. A universal range of ac input (90-230V), 48V dc output, 100W load, 100 KHz switching frequency integrated converter is implemented using MATLAB/ Simulink software. Experimental results conform and validate the analysis.

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Keywords: Charge current control; Integrated converter; PFC; Switched Mode Power Converter;

# 1. Introduction

Growing use of AC/DC power converters in industrial, transport, utility systems and home appliances introduces harmonic currents on low voltage AC public mains networks [1]. To minimize these harmonics and to meet IEC 6100-3-2 and other international regulations, the traditional method of using passive components network is not suitable for medium and high power levels due to increase in component size and lower efficiency [2]. Another method proposed in the past literature was active power factor correction technique [3]. The active power factor

\* Corresponding author. Tel.: +9885767652;

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E-mail address: subbarao.mopidevi@gmail.com

correction done with the help of simple single converter module is referred as single stage active power factor correction, but high current stress in switch and EMI problems makes it unattractive[4]. The next approach is two stage approaches, in which two separate converters are connected in cascade and out of two converters, one converter acts like a power factor correction converter and another acts as a voltage regulator. These two converters are controlled independently with two different controllers to realize the goal. Therefore it is expensive and more suitable for high power applications. This paper proposes an integration of converters approach which has the features of both single converter approach and two stage approaches.

Buck converter is integrated with flyback converter and named as integrated buck-flyback converter which is considered as the ISMPC in this paper[5-15]. The proposed converter operates as a flyback converter when input voltage is greater than buck capacitor voltage and as a buck converter when input voltage is less than buck capacitor voltage. It requires no dead zone, there by PF is improved and meets the IEC-61000-3-2 class C limits.

Charge control is a new and modern technique for PFC converters. In literature this controller was used in multi resonant and quasi resonant dc-dc converters [16, 17]. The origin of this controller is from the peak current controller, but having of features like using of external ramp is not required and better noise immunity.

### 2. Integrated Switched mode power Converter

In this buck converter is power factor correction converter and flyback converter as a power control converter. Buck Converter consists of  $L_b, D_c, D_a, SW_1, C_b, V_p$  and Flyback Converter consists of  $C_b, SW_1, 1:m, D_b, D_a, D_d, C_o$ . Here SW1 is common for both the converters.

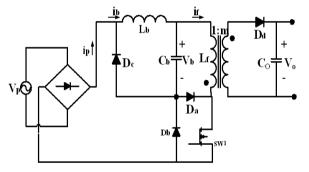


Fig. 1 Integrated Switched Mode Converter

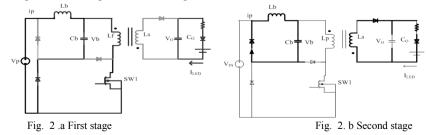
This converter operates in four stages,

First Stage: When SW1 is on, buck inductor  $(L_b)$  and flyback primary inductor  $(L_f)$  are storing energy and output capacitance (Co) feeding load.

Second Stage: When SW1 is off, buck inductor  $(L_b)$  is discharging and flyback secondary inductance is discharging.

Third Stage: before completion of discharge of flyback secondary inductor energy already buck inductor completes its energy completely.

Fourth Stage: In this flyback secondary inductor discharges energy completely and output capacitor feeds load. The above four stages of working is shown in Fig.2.



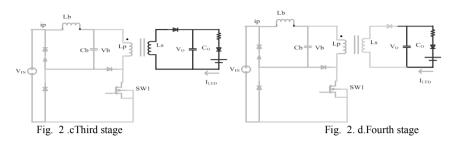


Fig. 2. Operation of ISMPC

#### 3. Charge Current Controlled ISMPC

Operation of charge control is particularly for Power factor correction converter is explained in this section. Fig.3 shows the circuit diagram of ISMPC with charge control is presented. At the starting of switching cycle, SW1 will be turn on and SW2 turnoff at same instant. SW1 current sensed and used to charge capacitor  $C_a$ . When capacitor voltage ( $V_{Ca}$ ) reaches to reference voltage  $V_r$ , SW1 will be turn off and SW2 will be turn on to discharge  $C_a$ . The voltage  $V_{Ca}$  is the total charge of the SW1 current in one cycle of switching period. The average value of SW1 current is proportional to switching period when the converter is operating with constant switching frequency.

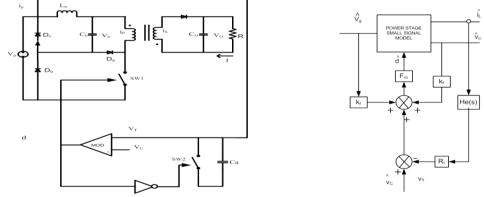


Fig. 3. Charge Current Controlled ISMPC



(1)

To analyze the performance of controller a small signal model of the current loop is derived and it's equivalent transfer function model is shown in Fig. 4. This integrated switch current expression in discrete form is,

$$I_s(Z) = -\frac{i_{s(DT_s)}}{D} z d(Z)$$

Its continuous time domain is,

$$I_{s}(S) = -\frac{i_{s(DT_{s})}}{D}e^{sTs}\frac{1-e^{-sTs}}{sTs}d(s)$$
(2)

The transfer function from the (2) is,

$$\frac{d(s)}{i_s(s)} = -G_m \ G_c H_e \ (s) \tag{3}$$

Where,

$$H_e(S) = \frac{ST_S}{e^{ST_{S-1}}}, \ G_m = \frac{D}{i_{s(DT_s)G_c}}$$

 $G_m$  is the modulator gain,  $G_c$  is the equivalent current gain and  $H_{e(s)}$  is the sample and hold effect.

To analyze stability of Converter need to study small signal model of converter with control to be develop, so the converter with controller transfer function is,

$$T_{C}(s) = G_{m} G_{c} G_{con}(s) H_{e}(s)$$
(4)

Where  $G_{con}(s)$  is the PFC converter transfer function.

$$G_{con}(s) = \frac{G_d}{1+sw_p}$$

$$G_d = \frac{2V_0 I_0}{D(V_0+I_0R_0)} , \quad w_p = \frac{(V_0+I_0R_0)}{C_0V_0R_0}$$
(5)

# 4. Design Example

Table.1 shows the some of the defined parameters. To meet IEC-1000-30-2 regulations the minimum conduction angle is  $130^{\circ}$  selected to achieve maximum powerfactor of 0.96 and % THD of 29% as in ref [9].

Value
90-265 V(R.M.S)
universal input range
48V
100 W
130 <sup>0</sup>
100 KHz

The voltage ratio (m) is calculated from the following relation;

$$m = \sin \frac{\pi - \theta}{2} = \frac{Vb}{Vp} = 0.4226$$
 (6)

Where  $\theta$  is the conduction angle,  $V_b$  is the bulk capacitor voltage,  $V_p$  is the peak value of line voltage.

In the universal line voltage range (90-265V) the minimum bulk capacitor voltage of 53V and maximum value rises up to 158V. In this design,

bulk capacitor voltage ( $V_b$ ) = 137V Flyback converter resistance  $(R_f) = \frac{V_b^2}{P_f} = \frac{137^2}{200/_{0.9}} = 84.46\Omega$ .  $L_b = _{178 \mu H}$  and  $L_f = _{754 \mu H}$  and Buck capacitor (C<sub>b</sub>) = 220  $\mu$ F.

### 5. Simulation and Experimental Results

#### 5.1. Simulation Results

Charge controlled integrated converter is implemented in MATLAB /Simulink. Fig 5. Shows the simulink model of converter.

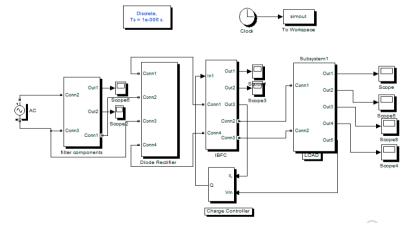


Fig. 5. MATLAB/Simulink model Charge Current controlled ISMPC.

Designed converter performance is verified for universal line voltage range at different load conditions .Fig.6.

Shows the source voltage and suorce current waveform for source voltage of 230V at rated load, it is observed that source voltage and currents are in phase. The calculated power factor is 0.94 and respective% THD line current is 20%.

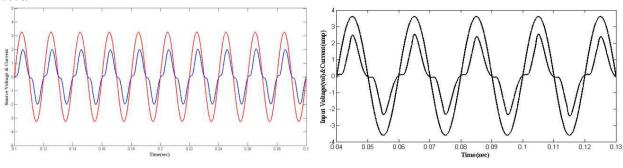


Fig. 6. Line voltage and current waveforms 230V(RMS)

Fig. 7. Line voltage and current waveforms 170V(RMS)

Converter is supplied with 170V at rated load the corresponding line voltage & line current waveform is shown in Fig.7. The power factor and %THD line current are 0.92 and 22%.

The Load voltage and load current wave forms are shown in Fig.8 and Fig.9.1t is observed that regulated load voltage of 48V is appeared across the load and load current of 2A.

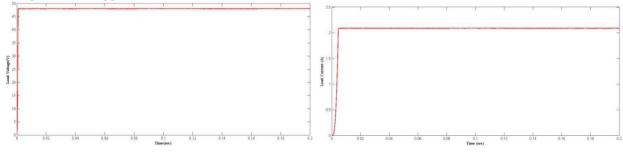


Fig. 8. Load voltage waveform

Fig. 9. Load current waveform

Load change is done on the converter at 0.2sec from rated load of 100W to 50W the converter giving the regulated voltage of 48V across the load terminals. This shows that converter operating effectively for load changes Fig.10 and Fig.11 shows the respective load current and voltage waveforms of the converter with load change.

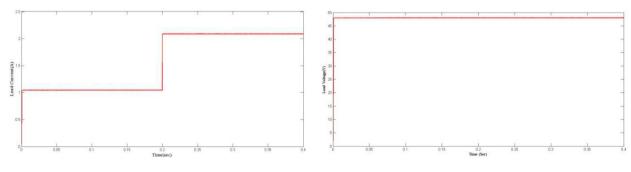


Fig. 10. Load current for step change of load at 0.2 sec.

Fig. 11. Load voltage for change of load at 0.2sec.

Fig.12 shows the bulk capacitor voltage is around 160V, which is low voltage as compared to two stage and single stage converters.

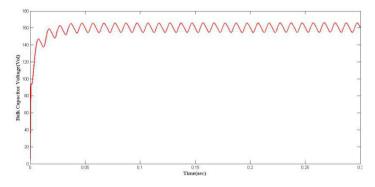


Fig. 12. bulk capacitor voltage waveform

In universal voltage range of voltage (90-230V) variation at rated load the % THD is shown in Table.2. The observed minimum power factor is 0.9 and maximum power factor is 0.94. Current THD range is from 27% to 20% which comply with IEC-61000-3-2.

V	%THD	Power Factor	V
V P	(Input Current)	(Input current)	<b>v</b> <sub>0</sub>
90	27%	0.9	48
110	24%	0.91	48
120	23%	0.91	48
150	22%	0.92	48
230	20%	0.94	48

Table2. The power factor and %THD with respect to universal line voltage range at rated load of 2A.

Table 3. The power factor and % THD with load variation at line voltage of 230V (RMS)

0/ I J	% THD	Power Factor	N/
% Load	(Input Current)	(Input Current)	Vo
20%	28%	0.9	48
40%	24%	0.91	48
60%	23%	0.92	48
80%	22%	0.93	48
100%	20%	0.94	48

#### 5.2. Experimental Results

Hardware setup was implemented in the laboratory as shown in the Fig.13 to investigate the performance of the charge current controller for the integrated buck-flyback converter. The components used in the experimental work are tabulated in Table 4.

rable 4. mardware components			
S.NO	Component Name	Symbol	Series number
1	Control Switch (Power IGBT)	SW1	FGA15N120ANTD
2	Power Diode	Dd	MUR3060PT
3	Power Diode	Da,Db,Dc	MUR3040PT

Table 4 Hardware components

Fig.14 and Fig.15 shows the source voltage and current waveforms at supply voltage of 170V,50Hz and 230V,50Hz at rated load. In Fig.16  $i_5$  is the load current waveform and  $v_5$  is the load voltage waveform. Fig.17. shows the bulk capacitor voltage waveform.

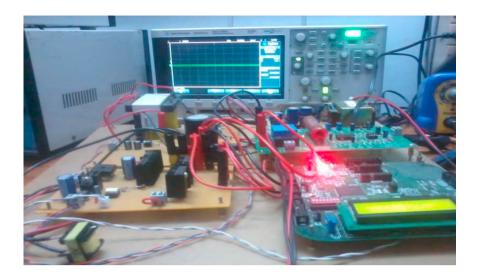


Fig. 13Hardware model of Proposed converter

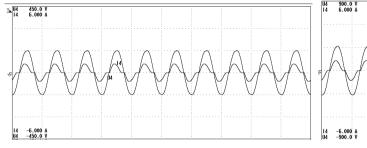


Fig. 14. Line voltage & current waveforms for 150V(RMS)

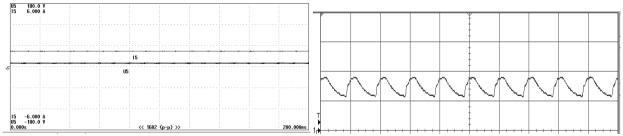


Fig. 16 Load voltage and load current waveforms

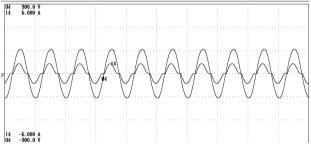
Fig. 17 Bulk capacitor voltage waveform

# Experimental and simulations comparative results are shown in Table 5.

	Simulation Results	Experimental Results
Input Voltage	230	229
Output Voltage	48	47.354
%THD	20	20.25
Power factor	0.94	0.938

# Table 5. Comparative results

Fig. 15 Line voltage & current waveforms for230V(RMS)





#### 6. Conclusion

Integrated switched mode power converter is designed by cascading buck converter with flyback converter because of having feature of current flowing through switch is either buck current or flyback current not sum of both currents, hence switch losses are reduced. Designed converter results are verified for different line and load conditions obtained lower value of power factor is 0.9 at low line voltage and reaches to 0.94 for 230V, highest percentage of THD is 27% and lowest percentage of THD is 20% and it meets the IEC-6100-3-2 norms for class-C and Class-D appliances. The proposed control scheme applied to the converter and implemented in MATLAB/ Simulink tool, their performance was evaluated both in steady state and dynamic conditions. Simulation and experimental results shows that controller acts quickly for load changes as shown in the load current waveform. Experimental results validate the satisfactory with simulation results.

#### References

- [1]SupratimBasu and Math.H.J.Bollen, "A Novel Common Power Factor Correction Scheme for Homes and Offices," IEEE Transactions on Power Delivery, Vol.20, No.3, pp. 2257-2263, July 2005.
- [2]Laszlo Huber, Jindong Zhang, Milan M. Jovanovic', and Fred C. Lee "Generalized Topologies of Single-Stage Input-Current-Shaping Circuits" IEEE Transactions on Power Electronics, Vol. 16, No. 4, July 2001.
- [3] JM.subbarao, et al., "Analysis and Design of Non-Isolated Single Phase AC/DC PFC Topologies to Drive LEDs," in proc. International Conference on Smart Electric Grid (ISEG), 2014.
- [4]Dylan Dah-Chuan Lu, Herbert Ho-Chinglu, and VeliborPjevalica, "A Single-Stage AC/DC Converter With High Power Factor, Regulated Bus Voltage, and Output Voltage", IEEE Trans. Power Electronics, Vol. 23, No. 1, pp. 218-228, Mar. 2008.
- [5]S.Busquest-Monge, J-C.Crebier, S.Ragon, E.Hertz, D.Boroyevich, Z.Guradal, M.Arpilliere, D.K.Lindner, "Design of a Boost power factor correction converter using optimization techniques", *IEEETrans. on Power Electronics*, Vol.19, No.6, pp.1388-1396, Nov. 2004.
- [6]L. Huber, L. Gang, and M. M. Jovanovic, "Design-oriented analysis and performance evaluation of buck PFC front end," IEEE Trans. Power Electron., vol. 25, no. 1, pp. 85–94, Jan. 2010.
- [7]B. Keogh, "Power factor correction using the buck topology—Efficiency benefits and practical design considerations," in *Proc. Texas Instrum. Power Supply Design Seminar (SEM)*, 2011.
- [8]J. M. Alonso, A. J. Calleja, J. Ribas, E. López, M. Rico, and J. Sebastián, "Using input current shaper in the implementation of high-powerfactor electronic ballasts," in *Proc. IEEE APEC* '99, Dallas, TX, 1999, pp.746–752.
- [9]J. M. Alonso, A. J. Calleja, J. Ribas, E. Corominas, and M. Rico, "Evaluation of a novel single-stage high-power-factor electronic ballast based on integrated buck half-bridge resonant inverter," in Proc. IEEE APEC '00, New Orleans, LA, 2000, pp. 610–616.
- [10]J. M. Alonso et al., "Reducing storage capacitance in off-line LED power supplies by using integrated converters," in Proc. IEEE Ind. Appl. Soc. Annu. Meeting (IAS), Las Vegas, NV, USA, Oct. 2012, pp. 1–8.
- [11]M. A. Dalla Costa, J. M. Alonso, T. B. Marchesan, M. Cervi, and R. N. Prado, "Generalized analysis and comparison of high-power-factor integrated topologies to supply metal halide lamps with low frequency square waveform," in *Proc. 42nd IAS Annu. Meeting, Conf. Rec. IEEE Ind. Appl. Conf.*, New Orleans, LA, USA, Sep. 2007, pp. 484–489.
- [12]T. B. Marchesan et al., "Integration methodology of DC/DC converters to supply HPS lamps: An experimental approach," in Proc. IEEE Ind. Appl. Soc. Annu. Meeting (IAS), Edmonton, AB, Canada, Oct. 2008, pp. 1–5.
- [13]M.SubbaRao, Dr. Ch.Sai Babu, Dr.S.Satynarayana," Analysis & Design of Peak Current Controlled IBFC for High power factor & Tight Voltage Regulation" at International Conference(ICAEE'14) on VIT university, vellorejan.2014.
- [14]M. T. Madigan, R. W. Erickson, and E. H. Ismail, "Integrated highquality rectifier-regulators," *IEEE Trans. Ind. Electron.*, vol. 46, no. 4, pp. 749–758, Aug. 1999.
- [15]M.SubbaRao, Dr.Ch.Sai Babu, Dr.S.Satynarayana, "LPCM Controlled Single Phase AC-DC Converter For High Power Factor & Tight Voltage Regulation" Journal of Electrical Engineering(JEE), Vol. 13, no.4, Dec. 2013, pp.230-236.
- [16] Zhiyuan Hu, Yan-Fei Liu and Paresh C. Sen, "Bang–Bang Charge Control for LLC Resonant Converters", *IEEE Trans. Power Electronics*, Vol. 30, no. 2, pp. 1093-1108, Feb. 2015.
- [17] W. Tang, F. C. Lee, R. B. Ridley, and I. Cohen, "Charge control: Modeling, analysis, and design," *IEEE Trans. Power Electron.*, vol. 8, no. 4, pp. 396–403, Oct. 1993.

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